

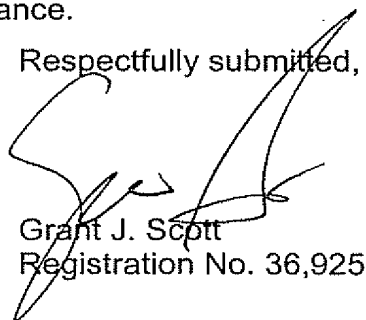
REMARKS

Applicants appreciate the examination of the application that is evidenced by the Official Action of June 21, 2006 and the indication that Claims 1-6 and 9-13 are allowed. In response to the Official Action, Claim 7 has been amended to include recitations from Claim 8, which was indicated as reciting allowable subject matter, and Claim 8 has been canceled. New Claim 14 has also been added. Applicants submit that Claim 14 is patentable at least per the patentability of the allowed claims.

Applicants submit that the amendments to Claim 7 are not to be treated as any acquiescence by Applicants that the Examiner's rejection of Claim 7 is properly supported by the cited prior art references. In particular, the Examiner's reliance on the '588 patent to Steinmetz et al. is believed to be improper because Steinmetz et al. provides no additional disclosure than already provided by Applicants' admitted prior art, which does not disclose or suggest the subject matter of original Claim 7. (See, e.g., FIG. 1A and pp. 4-5 of the present application). Applicants also believe the Examiner's reliance on the IDT datasheet ("3.3V CMOS Sync FIFO") is improper. As illustrated at page 24 and FIG. 31 of this IDT datasheet, the cascaded (i.e., series) arrangement of FIFO devices that support depth expansion only supports a collective FWFT mode of operation – not a standard mode of operation (see, e.g., p. 2 of the IDT datasheet for an explanation of differences between standard and FWFT modes of operation). Applicants acknowledge that FIG. 30 of the IDT datasheet discloses one form of depth expansion of multiple FIFO chips, but this depth expansion is not a "cascaded" form of depth expansion as recited by original Claim 7.

Based on the above amendments, Applicants respectfully submit that the present application is in condition for allowance.

Respectfully submitted,



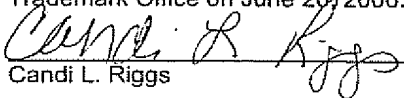
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